

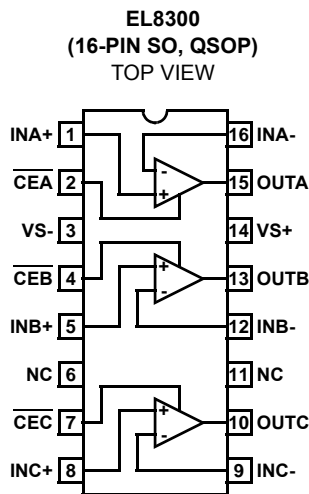
200MHz Rail-to-Rail Amplifier

The EL8300 represents a triple rail-to-rail amplifier with a -3dB bandwidth of 200MHz and slew rate of 200V/ μ s. Running off a very low supply current of 2mA per channel, the EL8300 also features inputs that go to 0.15V below the V_{S-} rail.

The EL8300 includes a fast-acting disable/power-down circuit. With a 25ns disable and a 200ns enable, the EL8300 is ideal for multiplexing applications.

The EL8300 is designed for a number of general purpose video, communication, instrumentation, and industrial applications. The EL8300 is available in an 16-pin SO and 16-pin QSOP packages and is specified for operation over the -40°C to +85°C temperature range.

Pinout



Features

- 200MHz -3dB bandwidth
- 200V/ μ s slew rate
- Low supply current = 2mA per amplifier
- Supplies from 3V to 5.5V
- Rail-to-rail output
- Input to 0.15V below V_{S-}
- Fast 25ns disable
- Low cost
- Pb-Free plus Anneal available (RoHS compliant)

Applications

- Video amplifiers
- Portable/hand-held products
- Communications devices

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL8300IS	16-Pin SO	-	MDP0027
EL8300IS-T7	16-Pin SO	7"	MDP0027
EL8300IS-T13	16-Pin SO	13"	MDP0027
EL8300ISZ (See Note)	16-Pin SO (Pb-free)	-	MDP0027
EL8300ISZ-T7 (See Note)	16-Pin SO (Pb-free)	7"	MDP0027
EL8300ISZ-T13 (See Note)	16-Pin SO (Pb-free)	13"	MDP0027
EL8300IU	16-Pin QSOP	-	MDP0040
EL8300IU-T7	16-Pin QSOP	7"	MDP0040
EL8300IU-T13	16-Pin QSOP	13"	MDP0040
EL8300IUZ (See Note)	16-Pin QSOP (Pb-free)	-	MDP0040
EL8300IUZ-T7 (See Note)	16-Pin QSOP (Pb-free)	7"	MDP0040
EL8300IUZ-T13 (See Note)	16-Pin QSOP (Pb-free)	13"	MDP0040

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage from V_{S+} to V_{S-}	5.5V	Power Dissipation	See Curves
Input Voltage	$V_{S+} + 0.3\text{V}$ to $V_{S-} - 0.3\text{V}$	Storage Temperature	-65°C to $+125^\circ\text{C}$
Differential Input Voltage2V	Ambient Operating Temperature	-40°C to $+85^\circ\text{C}$
Continuous Output Current	40mA	Operating Junction Temperature	$+125^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_{S+} = 5\text{V}$, $V_{S-} = \text{GND}$, $T_A = 25^\circ\text{C}$, $V_{CM} = 2.5\text{V}$, R_L to 2.5V, $A_V = 1$, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Offset Voltage		-5	-0.8	+5	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		3		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{IN} = 0\text{V}$	-3	-1.4		μA
I_{OS}	Input Offset Current	$V_{IN} = 0\text{V}$		0.2	0.55	μA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		2		$\text{nA}/^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	$V_{CM} = -0.15\text{V}$ to $+3.5\text{V}$	70	90		dB
CMIR	Common Mode Input Range		$V_{S-} - 0.15$		$V_{S+} - 1.5$	V
R_{IN}	Input Resistance	Common Mode		16		$\text{M}\Omega$
C_{IN}	Input Capacitance			0.5		pF
A_{VOL}	Open Loop Gain	$V_{OUT} = +1.5\text{V}$ to $+3.5\text{V}$, $R_L = 1\text{k}\Omega$ to GND	75	90		dB
		$V_{OUT} = +1.5\text{V}$ to $+3.5\text{V}$, $R_L = 150\Omega$ to GND		80		dB
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	$A_V = +1$		30		$\text{m}\Omega$
V_{OP}	Positive Output Voltage Swing	$R_L = 1\text{k}\Omega$	4.85	4.88		V
		$R_L = 150\Omega$	4.65	4.68		V
V_{ON}	Negative Output Voltage Swing	$R_L = 150\Omega$		150	200	mV
		$R_L = 1\text{k}\Omega$		50	65	mV
I_{OUT}	Linear Output Current			65		mA
$I_{SC}(\text{source})$	Short Circuit Current	$R_L = 10\Omega$	50	75		mA
$I_{SC}(\text{sink})$	Short Circuit Current	$R_L = 10\Omega$	90	130		mA
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	$V_{S+} = 4.5\text{V}$ to 5.5V	70	100		dB
I_{S-ON}	Supply Current - Enabled per Amplifier			2	2.6	mA
I_{S-OFF}	Supply Current - Disabled per Amplifier			40	90	μA
ENABLE						
t_{EN}	Enable Time			200		ns
t_{DS}	Disable Time			25		ns
V_{IH-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Power-up			0.8		V
V_{IL-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Shut-down			2		V

EL8300

Electrical Specifications $V_{S+} = 5V, V_{S-} = GND, T_A = 25^\circ C, V_{CM} = 2.5V, R_L \text{ to } 2.5V, A_V = 1$, Unless Otherwise Specified (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH-ENB}	ENABLE Pin Input Current High			8.6		μA
I_{IL-ENB}	ENABLE Pin Input for Current Low			0.01		μA
AC PERFORMANCE						
BW	-3dB Bandwidth	$A_V = +1, R_F = 0\Omega, C_L = 1.5pF$		200		MHz
		$A_V = -1, R_F = 1k\Omega, C_L = 1.5pF$		90		MHz
		$A_V = +2, R_F = 1k\Omega, C_L = 1.5pF$		90		MHz
		$A_V = +10, R_F = 1k\Omega, C_L = 1.5pF$		10		MHz
BW	$\pm 0.1dB$ Bandwidth	$A_V = +1, R_F = 0\Omega, C_L = 1.5pF$		20		MHz
Peak	Peaking	$A_V = +1, R_F = 1k\Omega, C_L = 5pF$		1		dB
GBWP	Gain Bandwidth Product			100		MHz
PM	Phase Margin	$R_L = 1k\Omega, C_L = 1.5pF$		55		$^\circ$
SR	Slew Rate	$A_V = 2, R_L = 100\Omega, V_{OUT} = 0.5V \text{ to } 4.5V$	160	200		V/ μs
t_R	Rise Time	$2.5V_{STEP}, 20\% - 80\%$		8		ns
t_F	Fall Time	$2.5V_{STEP}, 20\% - 80\%$		7		ns
OS	Overshoot	200mV step		10		%
t_{PD}	Propagation Delay	200mV step		2		ns
t_S	0.1% Settling Time	200mV step		20		ns
dG	Differential Gain	$A_V = +2, R_F = 1k\Omega, R_L = 150\Omega$		0.035		%
dP	Differential Phase	$A_V = +2, R_F = 1k\Omega, R_L = 150\Omega$		0.05		$^\circ$
e_N	Input Noise Voltage	$f = 10kHz$		10		nV/ \sqrt{Hz}
i_{N+}	Positive Input Noise Current	$f = 10kHz$		1		pA/ \sqrt{Hz}
i_{N-}	Negative Input Noise Current	$f = 10kHz$		0.8		pA/ \sqrt{Hz}
e_S	Channel Separation	$f = 100kHz$		95		dB

Pin Descriptions

PIN	NAME	FUNCTION
1, 5, 8	INA+, INB+, INC+	Non-inverting input for each channel
2, 4, 7	$\overline{CEA}, \overline{CEB}, \overline{CEC}$	Enable and disable input for each channel
3	VS-	Negative power supply
6, 11	NC	Not connected
9, 12, 16	INC-, INB-, INA-	Inverting input for each channel
10, 13, 15	OUTC, OUTB, OUTA	Amplifier output for each channel
14	VS+	Positive power supply

Typical Performance Curves

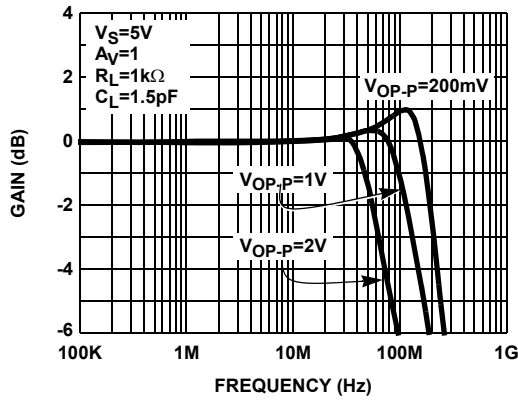


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGE LEVELS

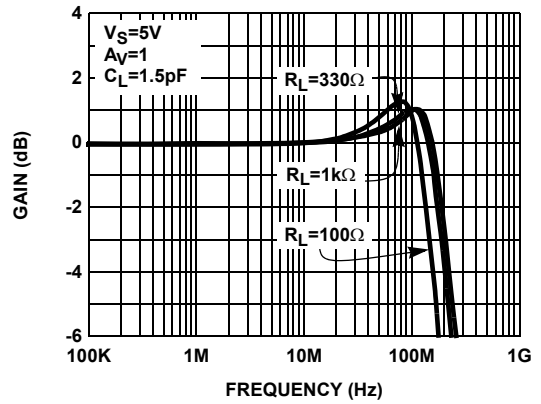


FIGURE 2. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS R_{LOAD}

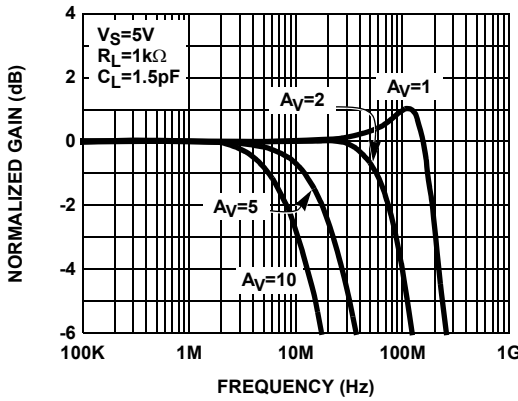


FIGURE 3. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS NON-INVERTING GAINS

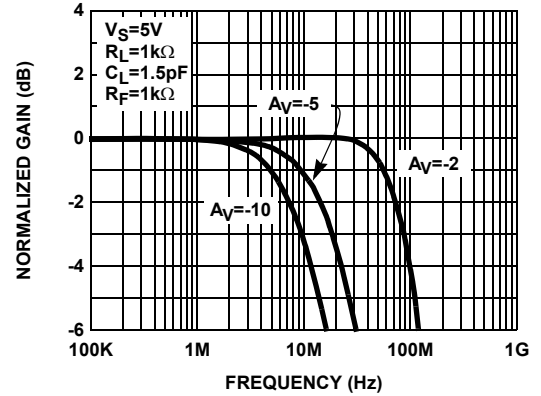


FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS INVERTING GAINS

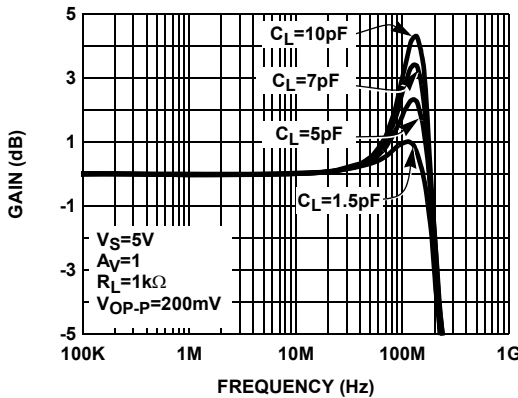


FIGURE 5. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS C_L

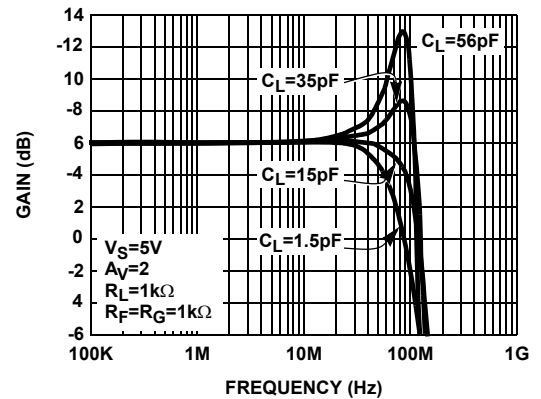


FIGURE 6. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS C_L

Typical Performance Curves (Continued)

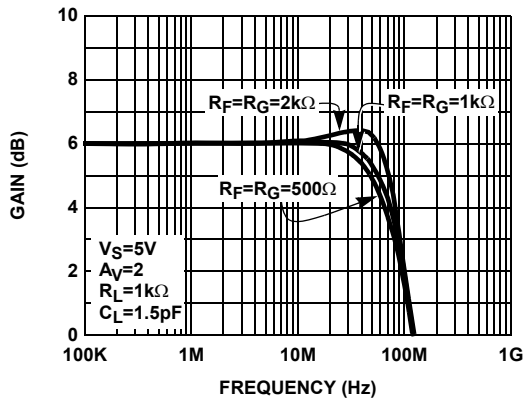


FIGURE 7. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS R_F AND R_G

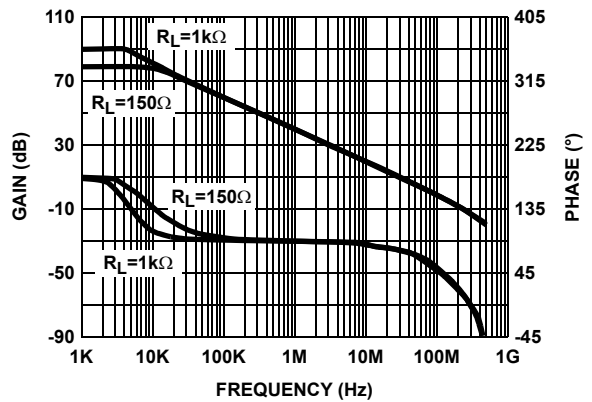


FIGURE 8. OPEN LOOP GAIN AND PHASE vs FREQUENCY

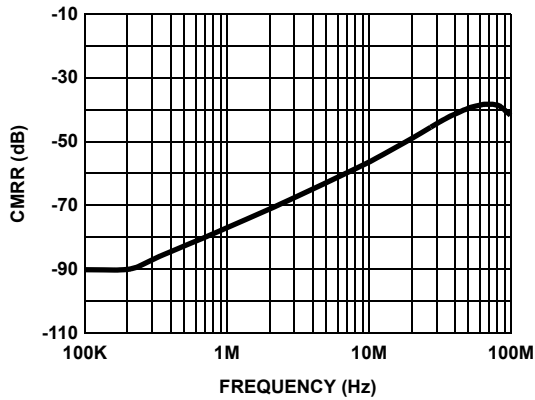


FIGURE 9. COMMON-MODE REJECTION RATIO vs FREQUENCY

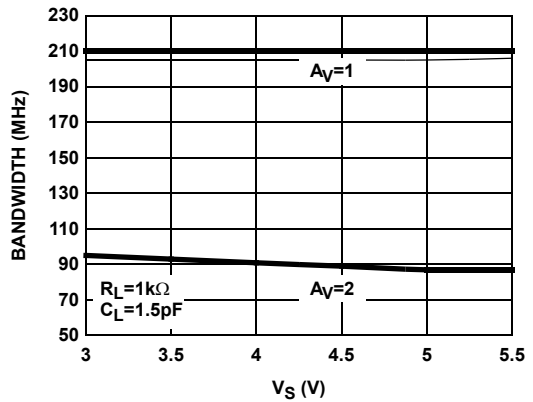


FIGURE 10. SMALL SIGNAL BANDWIDTH vs SUPPLY VOLTAGE

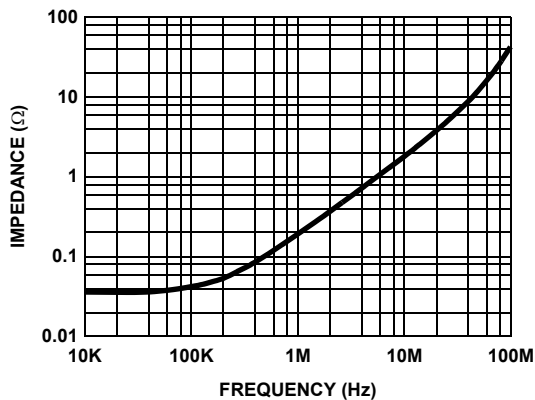


FIGURE 11. OUTPUT IMPEDANCE vs FREQUENCY

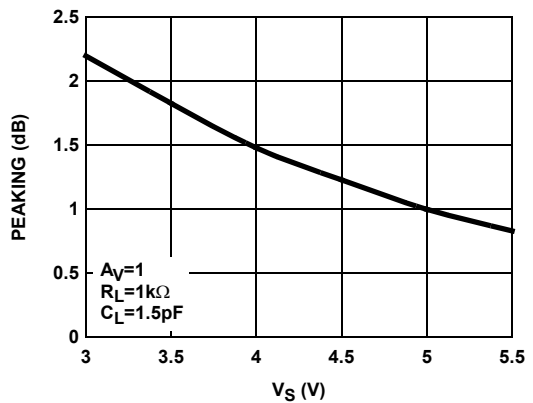


FIGURE 12. SMALL SIGNAL PEAKING vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

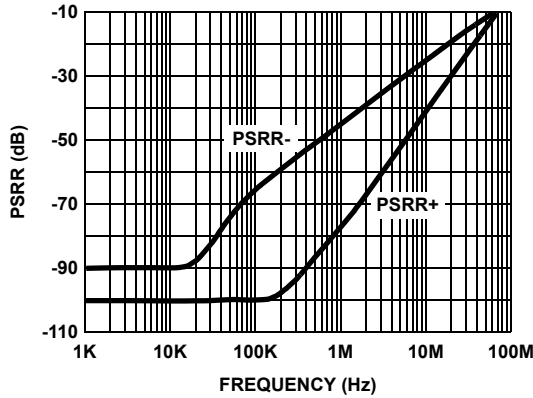


FIGURE 13. POWER SUPPLY REJECTION RATIO vs FREQUENCY

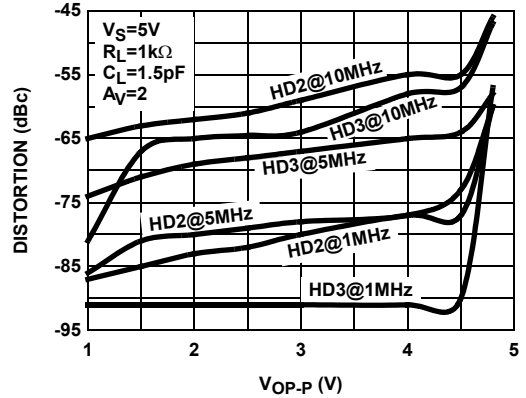


FIGURE 14. HARMONIC DISTORTION vs OUTPUT VOLTAGE

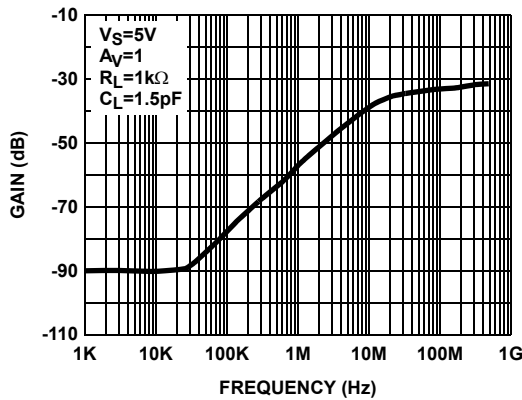


FIGURE 15. DISABLED OUTPUT ISOLATION FREQUENCY RESPONSE

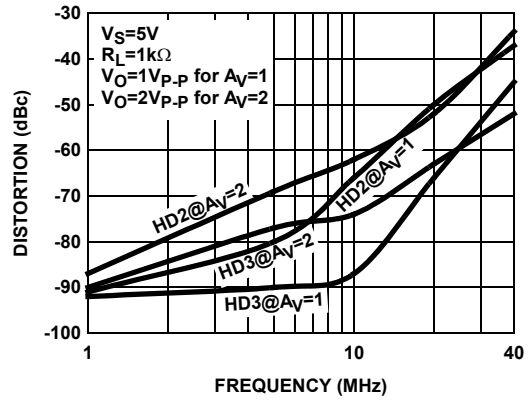


FIGURE 16. HARMONIC DISTORTION vs FREQUENCY

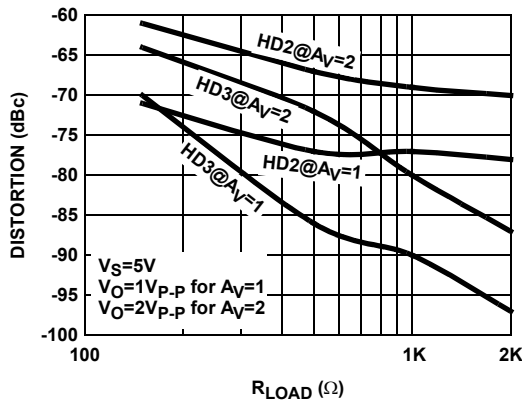


FIGURE 17. HARMONIC DISTORTION vs LOAD RESISTANCE

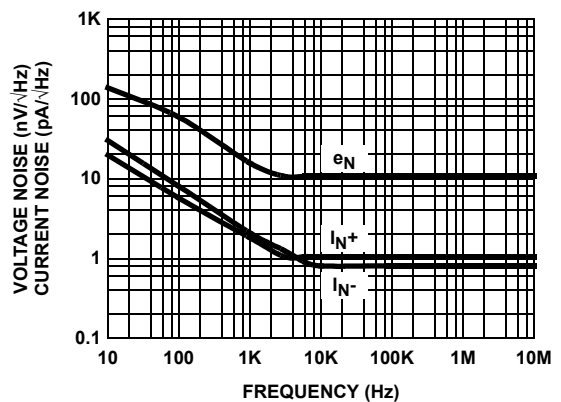


FIGURE 18. VOLTAGE AND CURRENT NOISE vs FREQUENCY

Typical Performance Curves (Continued)

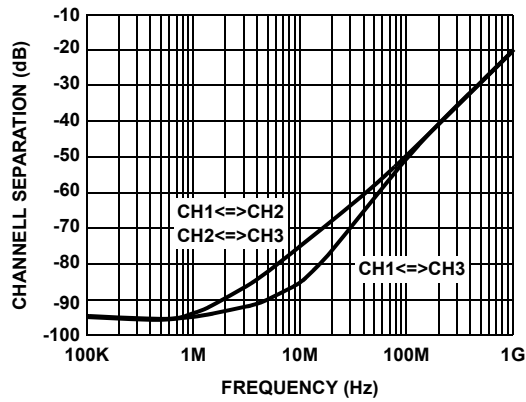


FIGURE 19. CHANNEL SEPARATION vs FREQUENCY

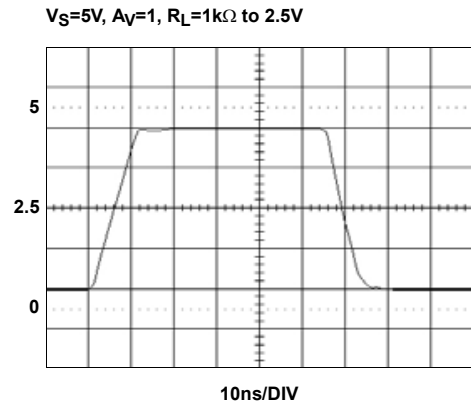


FIGURE 20. LARGE SIGNAL TRANSIENT RESPONSE

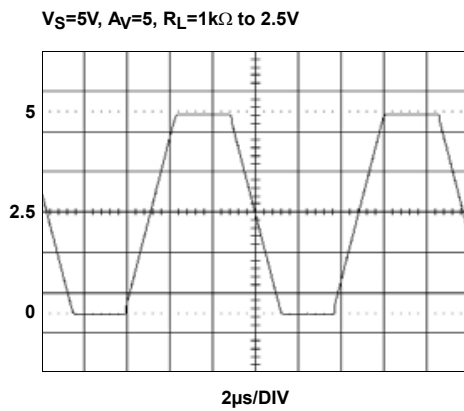


FIGURE 21. OUTPUT SWING

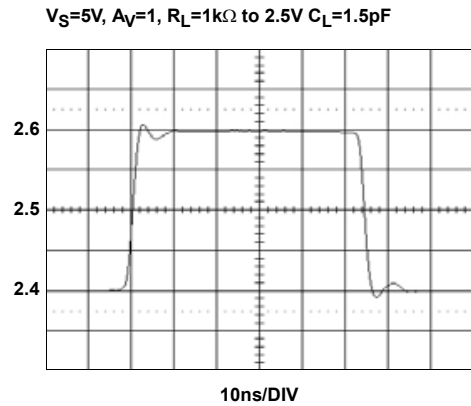


FIGURE 22. SMALL SIGNAL TRANSIENT RESPONSE

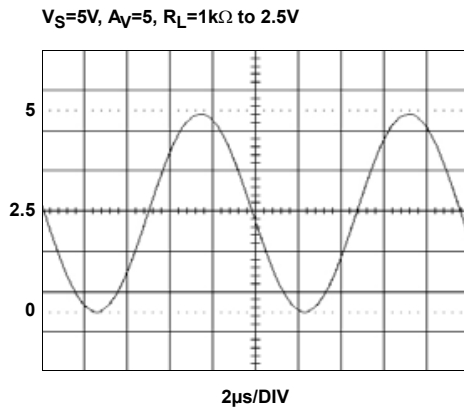


FIGURE 23. OUTPUT SWING

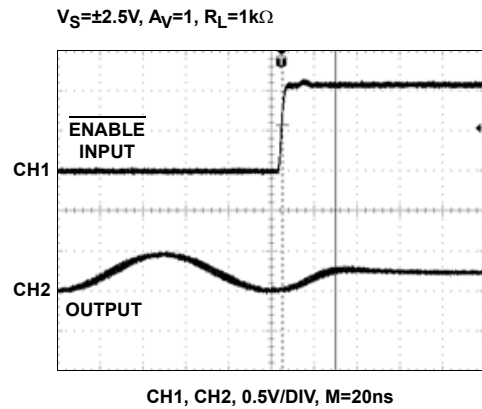


FIGURE 24. DISABLED RESPONSE

Typical Performance Curves (Continued)

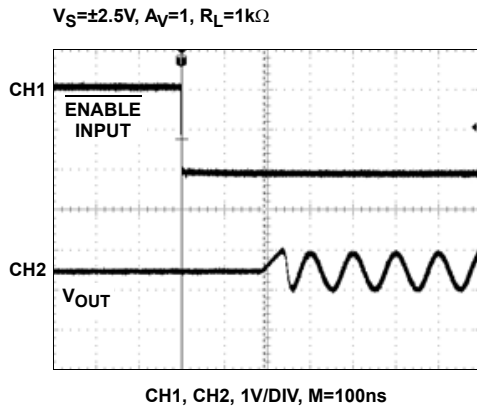


FIGURE 25. ENABLED RESPONSE

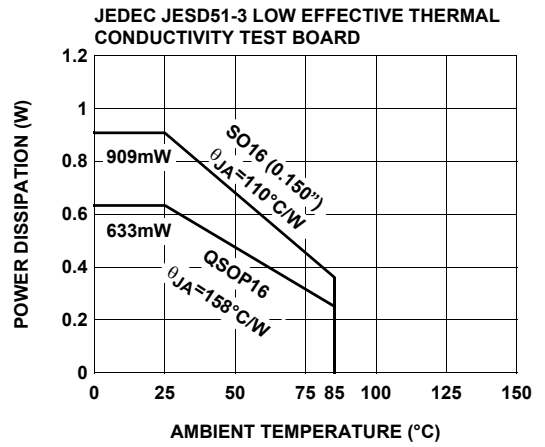


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

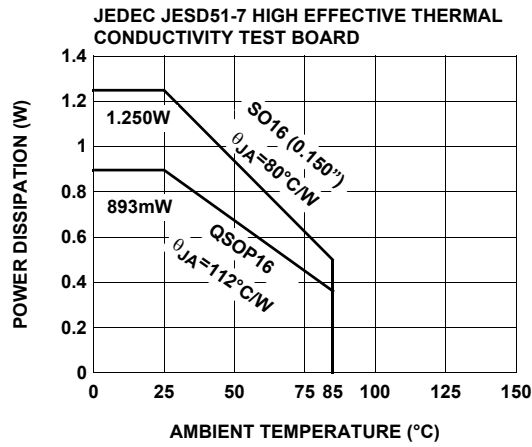


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Driving Capacitive Loads and Cables

The EL8100, EL8101 can drive 10pF loads in parallel with 1kΩ with less than 5dB of peaking at gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with the output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL8300 can be disabled and placed its output in a high impedance state. The turn off time for each channel is about 25ns and the turn on time is about 200ns. When disabled, the amplifier's supply current is reduced to 30μA typically, thereby effectively eliminating the power consumption. The amplifier's power down can be controlled by standard TTL or CMOS signal levels at the ENABLE pin. The applied logic signal is relative to V_{S-} pin. Letting the ENABLE pin float or applying a signal that is less than 0.8V above V_{S-} will enable the amplifier. The amplifier will be disabled when the signal at ENABLE pin is 2V above V_{S-}.

Output Drive Capability

The EL8300 does not have internal short circuit protection circuitry. They have a typical short circuit current of 70mA sourcing and 140mA sinking for the output is connected to half way between the rails with a 10Ω resistor. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±40mA. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the EL8300, it is possible to exceed the 125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^3 (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

For sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^3 (V_{OUTi} - V_{S-}) \times I_{LOADi}$$

Where:

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUTi} = Maximum output voltage of the application for each channel

R_{LOADi} = Load resistance tied to ground for each channel

I_{LOADi} = Load current for each channel

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOADi} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{S-} pin is connected to the ground plane, a single 4.7μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor from V_{S+} to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_{S-} pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Typical Applications

VIDEO SYNC PULSE REMOVER

Many CMOS analog to digital converters have a parasitic latch up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 28 shows a gain of 2 connections for EL8300. Figure 29 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

MULTIPLEXER

Besides the normal power down usage, the $\overline{\text{ENABLE}}$ pin of the EL8300 can be used for multiplexing applications. Figure 30 shows two channels with the outputs tied together, driving a back terminated 75Ω video load. A 2V_{P-P} 2MHz sine wave is applied to Amp A and a 1V_{P-P} 2MHz sine wave is applied to Amp B. Figure 31 shows the ENABLE signal and the resulting output waveform at V_{OUT}. Observe the break-before-make operation of the multiplexing. Amp A is on and V_{IN1} is passed through to the output when the ENABLE signal is low and turns off in about 25ns when the ENABLE signal is high. About 200ns later, Amp B turns on and V_{IN2} is passed through to the output. The break-before-make operation ensures that more than one amplifier isn't trying to drive the bus at the same time.

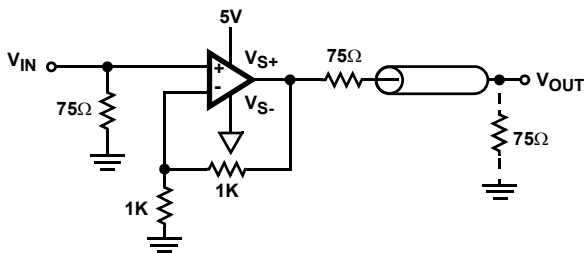


FIGURE 28. SYNC PULSE REMOVER

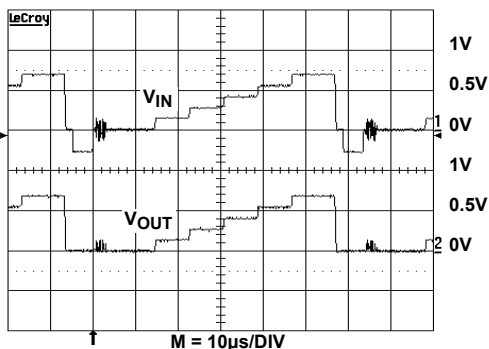


FIGURE 29. VIDEO SIGNAL

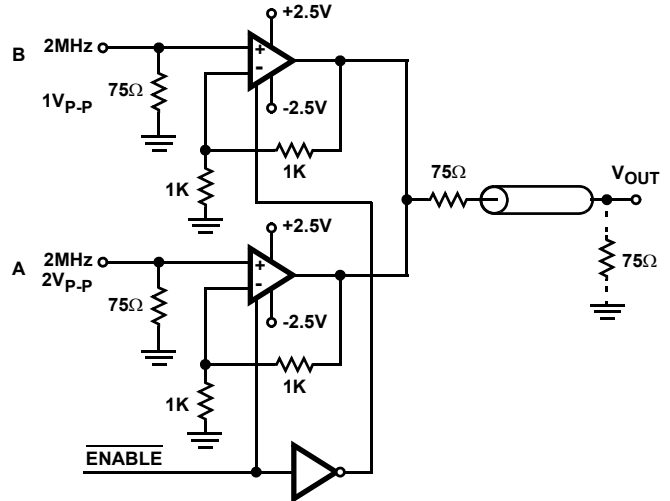


FIGURE 30. TWO TO ONE MULTIPLEXER

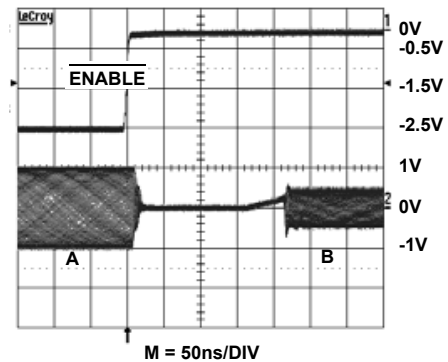


FIGURE 31. ENABLE SIGNAL

SINGLE SUPPLY VIDEO LINE DRIVER

The EL8300 is wideband rail-to-rail output op amplifiers with large output current, excellent dG, dP, and low distortion that allow them to drive video signals in low supply applications. Figure 32 is the single supply non-inverting video line driver configuration and Figure 33 is the inverting video line driver configuration. The signal is AC coupled by C₁. R₁ and R₂ are used to level shift the input and output to provide the largest output swing. R_F and R_G set the AC gain. C₂ isolates the virtual ground potential. R_T and R₃ are the termination resistors for the line. C₁, C₂ and C₃ are selected big enough to minimize the droop of the luminance signal.

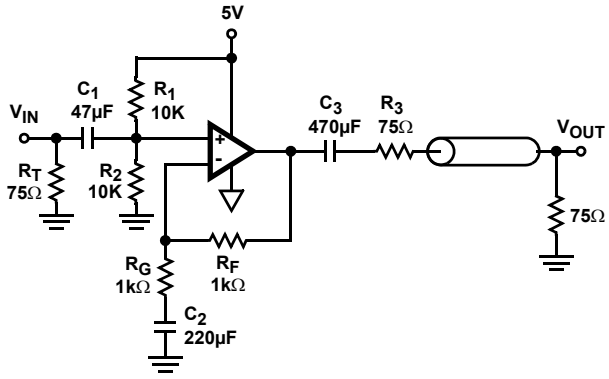


FIGURE 32. 5V SINGLE SUPPLY NON INVERTING VIDEO LINE DRIVER

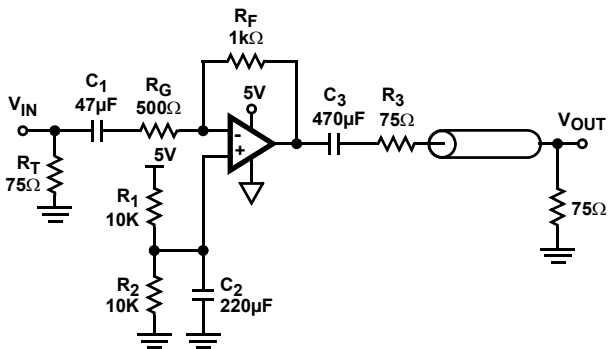


FIGURE 33. 5V SINGLE SUPPLY INVERTING VIDEO LINE DRIVER

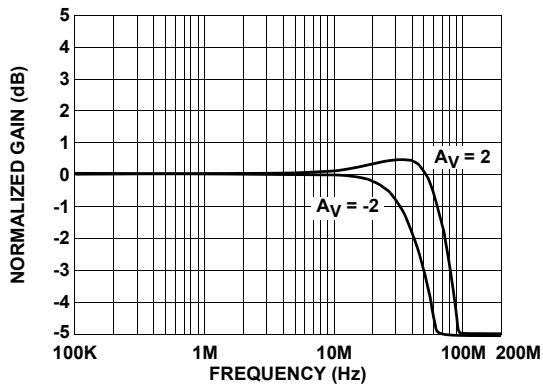
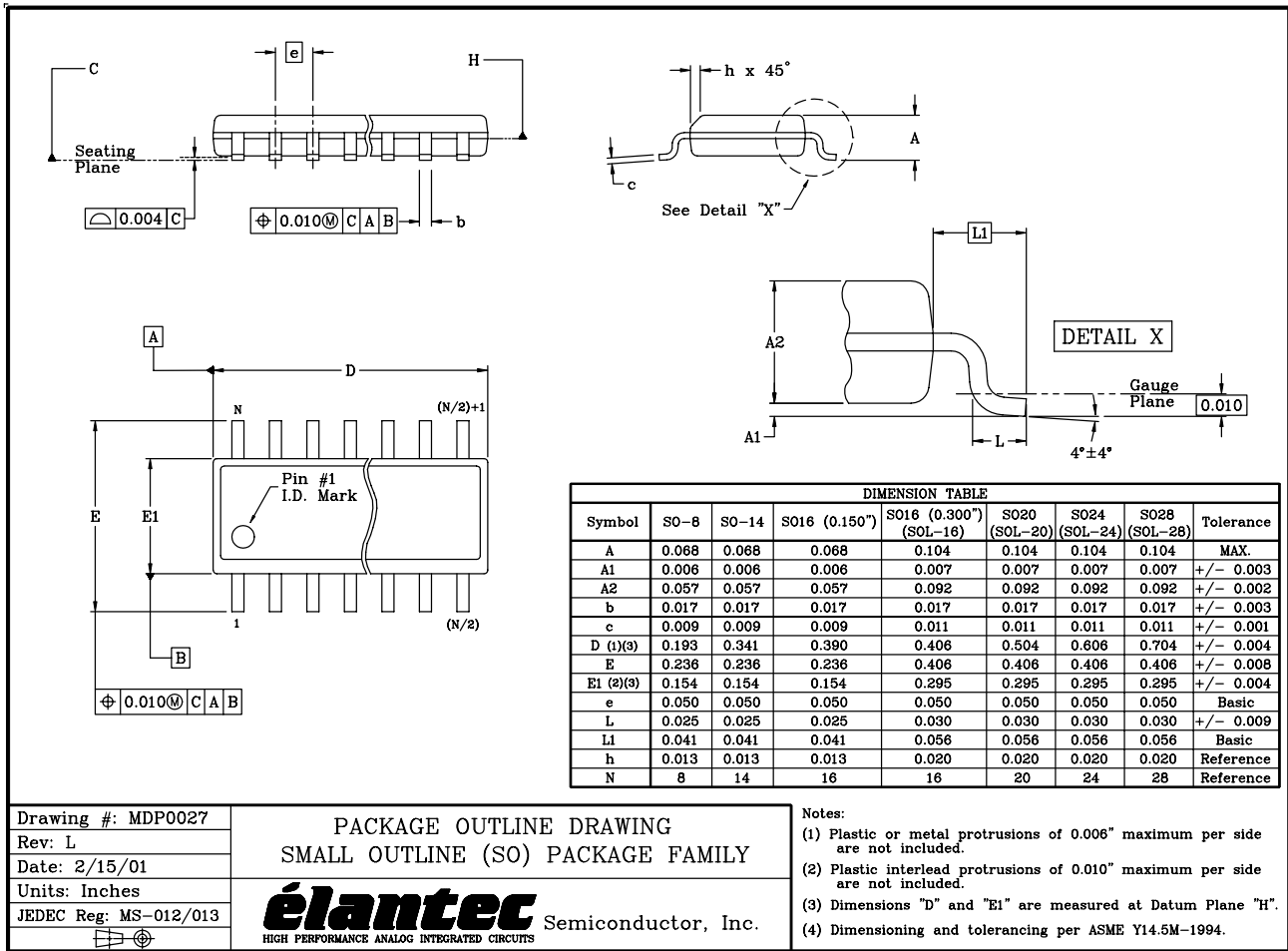


FIGURE 34. VIDEO LINE DRIVER FREQUENCY RESPONSE

SO Package Outline Drawing

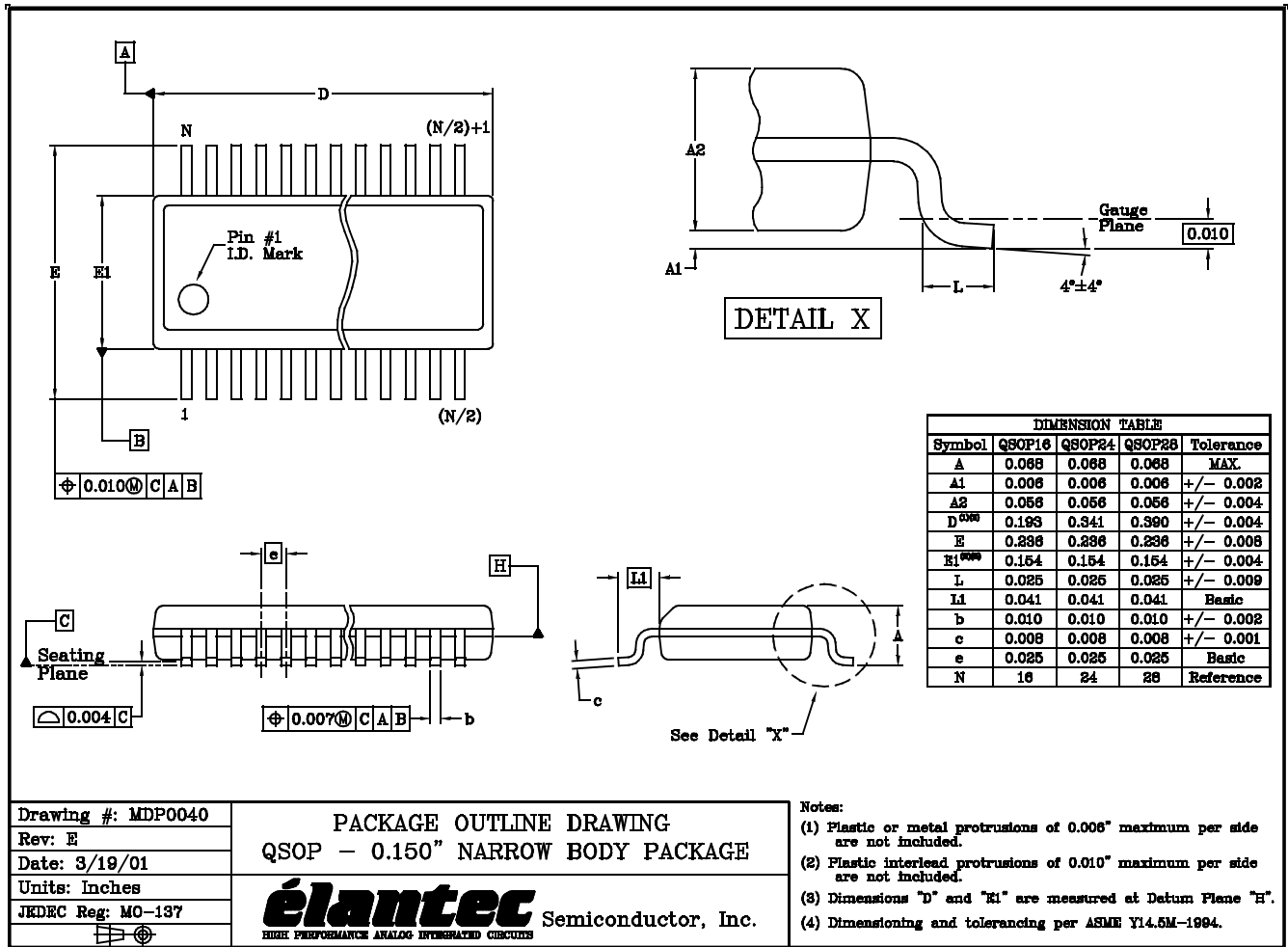


Drawing #: MDP0027
 Rev: L
 Date: 2/15/01
 Units: Inches
 JEDEC Reg: MS-012/013

PACKAGE OUTLINE DRAWING
 SMALL OUTLINE (SO) PACKAGE FAMILY

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QSOP Package Outline Drawing



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